BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, Pilani

KK Birla Goa Campus

INSTRUCTION DIVISION

FIRST SEMESTER 2024- 2025

COURSE HANDOUT (PART II)

Date: 28 / 07 / 2024

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No : EEE G626

Course Title : Hardware Software Codesign

Instructors/in-charge : Vipin Kizheppatt

1. Scope and Objective

The course provides advanced knowledge in the design of complex computer systems, in particular embedded systems. Models and methods are discussed that are fundamental for systems that consist of software and hardware components. Investigate topics ranging from system modeling to hardware-software implementation; explore analysis and optimization processes in support of algorithmic and architectural design decisions, and gain design experience with case studies using contemporary high-level methods and tools. The course emphasizes a top-down design methodology driven by bottom-up constraints.

2. Contents

The course covers the following subjects:

- Models for describing hardware and software components (specification)
- System design (hardware-software partitioning and design space exploration)
- Performance analysis and estimation techniques

3. Background

Basic knowledge in the following areas: computer architecture, digital design, software design, and embedded systems.

4. Textbook

1. Patrick R. Schaumont, A Practical Introduction to Hardware/Software Codesign, Springer, 2013
2. Ryan Kastner, Janarbek Matai, Stephen Neuendorffer, Parallel Programming for FPGAs- The HLS Book

5. Reference Book

1. Peter Marwedel, *Embedded System Design*, Springer 2003
2. Jorgen Staunstrup, Wayne Wolf, *Hardware / Software Co-Design: Principles and Practice*, Kluwer Academic, 1997.
3. Daniel D. Gajski, Samar Abdi, Andreas Gerstlauer and Gunar Schirner, Embedded System Design Modeling, Synthesis and Verification, Springer, 2009.
4. Xilinx User manuals

6. Course Plan

Lecture No.	Learning Objectives	Topics to be covered
01-02	Introduction	Introduction to Embedded System Design/High-Level Design, Introduction to Hardware/Software Codesign, Dualism of Hardware and Software designs.
03-10	FPGA-based System Design	Zynq Architecture Vivado IP Integrator flow Developing custom IP cores
10-21	Drivers and operating systems	Standalone operating system FreeRTOS operating system Petalinux Developing drivers for custom hardware
22-23	Co-simulation and Co-verification	Introduction to Co-simulation and Verification Environment
24-25	System on Chip (SoC) Hardware Software Platform	SoC Concepts, Design Principles of SoC Architectures
26-29	High-Level Synthesis	Introduction to High-level synthesis, Vitis HLS, HLS Pragmas, HLS interfaces
30-31	Design Quality Estimation	Quality Metrics, Hardware Estimation, Software Estimation
32-35	Codesign Examples	Video camera systems, Data dominated systems like DSP, CNN etc..

7. Evaluation Scheme

EC No.	Evaluation Component	Duration (min)	Weightage (%)	Date & Time	Nature of Component
1.	Mid Sem	1.5 hrs	20	8/10/23 (11:30-1:00)	Closed Book
2.	Lab/assignment	-	20	To be announced	Open Book
3.	Project and Viva	-	20	To be announced	Open Book
4.	Lab comprehensive	3 hrs	10	To be announced	Open Book
5.	Comprehensive	2 hrs	30	11/12/23 (AN)	Open Book

8. Lab

This course has lab components using Xilinx Vivado and Vitis software platform, and Zynq SoC platform

9. Chamber Consultation Hours

Tuesdays 4:30 – 5:30 PM

10. Notices

Notices regarding the course will be put up on the course web site (Quanta AWS)

11. Makeup

Make-up will be given on **genuine** grounds only. Prior application should be made for seeking the make- up examination.

Instructor - in - charge
EEE G626