Curriculum Vitae

Biju K Raveendran

Assistant Professor
Department of Computer Science & Information Systems
Faculty-in-charge, Computer Centre
BITS Pilani – K. K. BIRLA Goa campus
Goa – 403726, INDIA

Contact Information:

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URL: http://www.bits-pilani.ac.in/goa/biju/profile

Areas of Research Interest:

Operating Systems

Real time Embedded Operating systems: Energy efficient scheduling algorithms, Energy efficient memory management, File system design for Flash / Solid state devices, Preemptive I/O with priorities.

High performance Operating Systems: Multi-core / Multi – processor (MC/MP) scheduling, virtualization in MC/MP, Homogeneous and Heterogeneous MC/MP system for Real-time systems.

Low power Embedded Architecture

Energy efficient cache design; MC/MP architecture for real-time / embedded systems; Cache coherency issues of Multi – core system with scalable architectures.

Storage Systems

Energy efficient distributed file systems, energy efficient storage management with SAN and NAS.

P2P Overlay network

Mobile P2P for social networking, Delay tolerant networks

General Information:

Biju K Raveendran is with the Department of Computer Science and Information Systems at BITS Pilani K. K. BIRLA Goa campus since July 2009. Prior to this (July 2003 to June 2009), he worked with the Department of Computer Science and Information Systems at BITS Pilani, Pilani campus. He has about fifteen years of

research and teaching experience in the area of Operating Systems, Real-Time System and Computer Architecture.

For his PhD thesis, he worked on Energy Efficient Techniques for Multi-tasking Embedded Systems – Cache Design and Task Scheduling Algorithms under the guidance of Prof. S. Gurunarayanan. He was one of the five recipients of Microsoft Research India Fellowship in the year 2005 for his Ph.D. work. He is a recipient of Microsoft young faculty award in the year 2009. He developed a pseudo scheduler framework for Real-time Systems through which the administrator / system can select the scheduler at runtime. He designed Energy Efficient schedulers for RTLinux and Energy Efficient cache architectures for Embedded systems. These works were published in international forums.

He completed a project to architect and develop a programmer friendly development environment for Real-time / Embedded systems under Microsoft grant. He has done a project for Aditya Birla Group of Companies to model and design a framework for social networking infrastructure on mobile devices using P2P overlays. This project aims at designing scalable and customizable social networks that are mobile centric with minimum centralized infrastructure. He is also doing a project on Design and Implementation of High Performance Energy Efficient Scheduling Algorithms for Multiprocessor / Multicore Hard real – time systems. This project aims at designing and implementing hard real time scheduling algorithms with load balancing, processor shutdown and processor voltage and frequency scaling.

His major research focuses are energy efficiency in real-time / embedded scheduling, predictable and dependable real-time / embedded systems, Memory models – TLB, Caches and Main memory – for deterministic real-time systems, secondary storage / remote storage for real-time / embedded system and multi-core / multi-processor issues in real-time / embedded processors. 5 Ph.D. students are being guided / co-guided currently by him in the area of real-time / embedded system. Dr. Biju has undertaken significant R&D projects especially in the area of real-time / embedded systems. He also has research interest in the area of storage systems specifically Energy Efficiency of RAID, SAN, NAS and iSCSI. He is also active in the area of mobile P2P for social networks and delay tolerant networks.

He has been teaching courses on Operating systems, Advanced Operating Systems, Computer Architecture, Computer Organization, Advanced Computer Organization, Real – time systems, Software for Embedded systems, Data Storage

Technologies and Networks, Computer Programming I and Computer Programming II.

He received Microsoft Young Faculty Award in 2009. He was felicitated with "Best faculty award" by BITS Alumni Association (BITSAA) in the year 2013. He was one of the nucleus members of Admissions team who conducted first BITSAT online entrance examination successfully. He worked as a nucleus member of Information Processing Centre (IPC). He worked as a nucleus member of Computer Assisted Housekeeping unit (CAHU). He is currently working as Faculty – in – charge of Computer Centre, BITS Pilani K K BIRLA Goa campus. He is also serving as a member of Mission 2015 Technology Enablement imperative team.

Personal Information:

Name: Biju K Raveendran

Date of Birth: 26th March 1978

Nationality: INDIAN

Sex: Male

Marital Status: Married

Address for Communication:

A – 413,
Department of Computer Science & Information Systems
BITS Pilani K. K. BIRLA Goa campus,
Near NH 17B Bypass Road,
Zuarinagar, South Goa,
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URL: http://www.bits-pilani.ac.in/goa/biju/profile

Areas of Research Interest:

Operating System (OS): Real time Embedded OS: Energy efficient scheduling algorithms, Energy efficient memory management, File system design for Flash / Solid state devices, Preemptive I/O with priorities.

High performance OS: Multi-core / Multi – processor (MC/MP) scheduling, virtualization in MC/MP, Homogeneous and Heterogeneous MC/MP system for Real-time systems.

Low power Embedded Architecture: Energy efficient cache design; MC/MP architecture for real-time / embedded systems; Cache coherency issues of Multi – core system with scalable architectures.

Storage Systems: Energy efficient distributed file systems, energy efficient storage management with SAN and NAS.

P2P Overlay network: Mobile P2P for social networking, Delay tolerant networks

Education:

Ph.D. Computer Science (2009), BITS Pilani (Guide: Prof. S. Gurunarayanan)

Ph.D. Thesis Title: Energy Efficient Techniques for Multi-tasking Embedded Systems – Cache Design and Task Scheduling Algorithms

Teaching Record:

July 2003 – June 2004:	Assistant Lecturer, BITS Pilani, Pilani campus
July 2004 – Dec 2005:	Lecturer, BITS Pilani, Pilani campus
July 2009 – Till date:	Assistant Professor, BITS Pilani, K. K. BIRLA Goa campus

Administrative Experience:

July 2003 – June 2004:	Nucleus member, Information Processing Unit
July 2004 – Dec 2005:	Nucleus member, Admissions Unit
July 2009 – Dec 2013:	Nucleus member, Computer Assisted House Keeping Unit
Jan 2014 – Till date:	Faculty – in – charge, Computer Centre

Assignments handled in Department / Institute:

2009 – Till date:	Member, Doctoral Advisory Committee, for two Ph.D. students
2012 – 2015:	Convener, Doctoral Research Committee, Dept. of Computer Science & Information Systems
2013 – Till date:	Member, Mission 2015 Technology Enablement imperative team

Research Papers:

Biju Raveendran, Kajal Verma, Geeta Patil, "DTLB: Deterministic TLB for Tightly Bound Hard Real-time Systems", 2016 IEEE International Conference on Smart Systems and Technologies (SST 2016), 12 – 14 October 2016, Croatia [Accepted for Publication].

Biju Raveendran, Parag Panda, Geeta Patil, "A Survey on Replacement Strategies in Cache Memory for Embedded Systems", 2016 IEEE International Conference on Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER 2016), 13 – 14 August 2016, INDIA [Accepted for Publication].

Biju Raveendran, Mayuri Digalwar, Praveen Gahukar, Sudeept Mohan, "Energy Efficient Real Time Scheduling Algorithm for Mixed Task Set on Multi-core Processors", International Journal of Embedded Systems [Accepted for Publication].

Biju Raveendran, Shubhangi K Gawali, "DPS: A Dynamic Procrastination Scheduler for Multi-core/Multi-processor Hard Real Time Systems", in Proceedings of the 3rd IEEE International Conference on Control, Decision and Information Technologies (CoDIT'16), April 2016, Malta.

Biju Raveendran, Neethu Bal Mallya and Geeta Patil, "Simulation based Performance Study of Cache Coherence Protocols", in Proceedings of IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), December 2015.

Biju Raveendran, Mayuri Digalwar, Pravin Gahukar and Sudeept Mohan, "STREAM: A Simulation Tool for Energy Efficient Real Time Scheduling and Analysis", in Proceedings of the 6th International Workshop on Analysis

Tools and Methodologies for Embedded and Real-Time Systems (WATERS), July, 2015, Lund, Sweden.

Biju Raveendran, Neethu Bal Mallya and Geeta Patil, “Way Halted Prediction Cache: An Energy Efficient Cache Architecture for Embedded Processors”, in Proceedings of the 28th International Conference on VLSI design, January 2015.

Biju Raveendran, Chaitanya Datye and Sahil Deshpande, “LazyEDF: A Leakage Aware DVFS Scheduler for Periodic Hard Real-time Tasks”, in Proceedings of the IEEE International Conference on ICIIS, December 2014.

Biju Raveendran, Prashasti Baid, Prashanth S, “LLFRP: An Energy Efficient Variant of LLF with Reduced Pre-emptions for Real - Time Systems”, GSTF Journal on Computing (JoC) 3.4 (Apr 2014): 70-81.

Biju Raveendran, Mayuri Digarwar and Sudeept Mohan, “Dynamic Voltage and Frequency Scaling Algorithm for Mixed Task set”, in Proceedings of the 8th IEEE International Conference on ICISS, December 2013.

Biju Raveendran, Mayuri Digarwar and Sudeept Mohan, “Energy Aware Real-time Scheduling Algorithm for Mixed Task set”, in Proceedings of the International Conference on Advanced Electronic Systems, August 2013.

Biju Raveendran, Sundar Balasubramaniam and S. Gurunarayanan, “Evaluation of Priority Based Real Time Scheduling Algorithms: Choices and Tradeoffs”, in Proceedings of the 23rd Annual ACM Symposium on Applied Computing, pp. 302-307, March 2008.

Biju Raveendran, T S B Sudarshan, Avinash Patil, Komal Randive and S Gurunarayanan, “Predictive Placement Scheme for Set-Associative Cache

for Energy Efficient Embedded System", in Proceedings of International Conference on Signal Processing, Communications and Networking, pp. 152-157, January 2008.

Biju Raveendran, T S B Sudarshan, Dlip Kumar, Priyanaka Tugudu and S Gurunarayanan, "LLRU: Late LRU Replacement Strategy for Power Efficient Embedded Cache", in Proceedings of 15th IEEE International Conference on Advanced Computing and Communications, pp. 339-344, December 2007.

Biju Raveendran, T S B Sudarshan, Avinash Patil, Komal Randive and S Gurunarayanan, "An Energy Efficient Selective Placement Scheme for Set-Associative Data Cache in Embedded System", in Proceedings of ESA'07- The 2007 International Conference on Embedded Systems and Applications, pp. 188 – 194, June 2007.

Biju Raveendran, J P Misra, Karan Bhatnagar and S Gurunarayanan, "EFFS: Efficient Flash File System for Wireless Sensor Nodes", in Proceedings of ESA'07- The 2007 International Conference on Embedded Systems and Applications, pp. 159 – 165, June 2007.

Biju Raveendran, T S B Sudarshan S Gurunarayanan, "Selective Placement Data Cache for Low Energy Embedded System", in Proceedings of 14th IEEE International Conference on Advanced Computing and Communications, pp. 473-476, December 2006.

Biju Raveendran, Sundar Balasubramaniam, K Durga Prasad and S. Gurunarayanan, "Variants of Priority Scheduling Algorithms for Reduced Context Switches in Real Time System", in Proceedings of the 8th International Conference on Distributed Computing and Networking, Lecture Notes in Computer Science, pp. 466-478, December 2006.

Biju Raveendran , Sundar Balasubramaniam , K Durga Prasad and S. Gurunarayanan, “A Context-Switch Reduction Heuristic for Power-Aware Off-line Scheduling”, in Proceedings of the 11th Asia-Pacific Computer Systems Architecture Conference, Lecture Notes in Computer Science, pp. 404-411, September 2006.

Biju Raveendran, T S B Sudarshan, and S Gurunarayanan, “Cache Memory Design with Late Replacements for Embedded Systems”, in Proceedings of 2nd International Conference on Embedded Systems, Mobile Communication and Computing, pp 76-90, August 2006.

Projects

Sponsored Projects:

- To Architect and Develop a Programmer friendly development environment for Real-time / Embedded systems under Microsoft grant (2004 – 2006)
- To Model and Design Framework for Social Networking Infrastructure on Mobile Devices using P2P overlays – Aditya Birla Group of companies (2012 – 2013)
- To Design and Implementation of High Performance Energy Efficient Scheduling Algorithms for Multiprocessor / Multicore Hard Real-time Systems – Seed Grant (2013 – 2015)
- “Addressing Challenges in Application Development for Heterogeneous Computing Platform for Speedup and Power Efficiency” – DST (on going)

Courses Taught:

BITS C323/C324: Study Oriented Project
BITS C331/C335: Computer Project
BITS C412T: Under Graduate Thesis
BITS G540: Research Practice
BITS G553: Real – time Systems (Course capacity – 12)
BITS G620: Professional Practice I

BITS G621: Professional Practice II
BITS G629T: Post Graduate Dissertation
CS C342: Advanced Computer Organization (Course capacity – 220/180)
CS C342L: Data Structure and Algorithms Lab (Course capacity – 80)
CS C372: Operating Systems (Course capacity – 220/180)
CS C422: Parallel Computing (Course capacity – 50)
CS C424: Software for Embedded Systems (Course capacity – 20)
CS C446: Data Storage Technologies and Networks (Course cap – 30)
CS C491: Special Projects (Computer Science)
CS F111: Computer Programming (Course capacity – 600)
CS F342: Computer Architecture (Course capacity – 180)
CS F446: Data Storage Technologies and Networks (Course cap – 30)
CS G523: Software for Embedded Systems (Course capacity – 20)
CS G524: Advanced Computer Architecture (Course capacity – 12)
CS G562: Advanced Architecture and Performance Evaluation (CC – 20)
CS G623: Advanced Operating Systems (Course capacity – 12)
IS C351: Computer Organization and Architecture (Course cap – 60/50)
IS C362: Operating Systems (Course capacity – 60/50)
IS C411: Information Systems Project
IS C422: Parallel Computing (Course capacity – 50)
IS C424: Software for Embedded Systems (Course capacity – 20)
IS C446: Data Storage Technologies and Networks (Course cap – 20)
IS F241: Computer Organization (Course capacity – 50)
IS ZC362: Operating Systems – WILP (Course capacity – 250/100)
IS ZC424: Software for Embedded Systems (Course capacity – 200)
SS G523: Software for Embedded Systems (Course capacity – 20)
TA C162: Computer Programming I (Course capacity – 100/400/600)
TA C252: Computer Programming II (Course capacity – 100)

Semester wise break up:

Year	Semester I	Semester II
2016 - 2017	CS F342, CS G623	
2015 – 2016	CS F342, CS G623	CS F446, CS G524
2014 – 2015	CS F342, CS G623	CS F446, CS G524

2013 – 2014	CS F342, CS G523/SS G523	CS F446, CS F111 (2)
2012 – 2013	CS C372/IS C362, CS G523/SS G523	IS F241, CS G523/SS G523
Summer	Content Development – Systems Programming	
2011 – 2012	CS C372/ IS C362, CS C446 / IS C446	CSC342, CS C446 / IS C446
2010 – 2011	CS C372/ IS C362, IS ZC362, IS C351	IS ZC362, TA C162
2009 – 2010	BITS G553, TA C252	CS C342, TA C162
2008 – 2009	CS C372, TA C252	CS C342, CS G562
2007 – 2008	CS C372, TA C252	CS C342, CS C422 / IS C422
2006 – 2007	CS C372, TA C252	IS C362, TA C162
2005 – 2006	CS C372, BITS G553	IS C362, TA C162
2004 – 2005	CS C372, IS ZC362	IS ZC424, CS C424 / IS C424
2003 – 2004	CS C342L, CS C372	IS C362, TA C162

Ph.D. Thesis currently supervising:

As Supervisor:

1. **Ms. Shubhangi K Gawali**
   [Title: Design of High Performance Energy Efficient Scheduling Algorithms for Uniprocessor and MP/MC Hard Real-time Systems]
2. **Ms. Geeta Patil**
   [Title: Design of Energy Efficient Cache Architecture for Uniprocessor and Multicore Systems]
3. Mr. Arun S Nair
   [Title: Mixed Criticality Real-time Systems]
4. Ms. Julieta Luiza Louella M Mesquita
   [Title: Mixed Criticality Real-time Systems]

As Co-Supervisor:

1. **Ms. Mayuri Abhijeet Digalwar**
   [Title: Design and Implementation of some High Performance Thread Scheduling Algorithms for Heterogeneous MC processors]

Post Graduate Dissertation Supervised:

1. **Mr. Prashanth S [M.E. Embedded Systems – 2012]**
   [Title: Design of Energy Efficient Scheduling Algorithms for Real–time Operating Systems]
2. **Ms. Rachana A [M. E. Embedded Systems – 2012]**
   [Title: Performance Evaluation of Various Cache Replacement Policies]
3. **Mr. Santhosh Reddy V [M. E. Software Systems - 2012]**
   [Title: Energy Efficient Storage Systems]
4. **Mr. Siva Sai Ram Prasad K [M. E. Software Systems – 2013]**
   [Title: A Study on Various Optimizations of Multi-programming with Threads and Processes]
5. **Ms. Divya Vipin [M. E. Embedded Systems – 2014]**
   [Title: Performance Enhancement in Embedded Heterogeneous Multi-core Architecture using Cache Coherence Protocol and Optimal Load Balancing]
6. **Ms. Shweta Agrawal [M. E. Software Systems – 2014]**
   [Title: Design of Energy-Efficient Scheduling Algorithms for Multi-processor/Multi-core Hard Real-time Systems]
7. **Ms. Neethu Bal Mallya [M. E. Software Systems – 2015]**
   [Title: Design of Energy-Efficient Multi-core/Multi-processor Hard Real-time Systems]
8. **Prasanth [M. E. Computer Science – 2016]**
   [Title: Energy-Efficient Scheduling of Multi-core/Multi-processor Hard Real-time Systems]
9. **Alen K Sabu [M. E. Computer Science – 2016]**
   [Title: Performance Improvement of Multi-core Scheduler in Homogeneous and Heterogeneous Systems]

Under Graduate Thesis Supervised:

1. **Ms. Rituparna Ghosh [B.E. Computer Science – 2016]**
   [Title: Preemptive Heterogeneous Multi-processor Scheduling of Mixed Criticality Systems]
2. **Mr. Sahil Mittal [MSc. Tech Information Systems – 2015]**
   [Title: Design of Efficient Scheduling Algorithm for Heterogeneous Distributed Systems]
3. **Mr. Pravin Joshi [MSc. Tech Information Systems – 2015]**
   [Title: Design of Efficient Memory Management Scheme for Heterogeneous Distributed Systems]
4. **Ms. Prachi Shukla [MSc. Tech Information Systems – 2012]**
   [Title: Energy Efficient Multi-core Architecture]
5. **Mr. Karan Bhatnagar [MSc. Tech Information Systems – 2008]**
   [Title: Energy Efficient Flash File System for Embedded Devices]
6. **Mr. Durga Prasad [MSc. Tech Information Systems – 2006]**
   [Title: A Context Switch Reduction Heuristic for Real–time Scheduler]

Under Graduate Project students:

1. **Mr. Hari S R [B. E. Computer Science – 2016]**
   [Area: Mixed Criticality Systems]
2. **Mr. Gokul Dinesh [B. E. Computer Science – 2016]**
   [Area: Mixed Criticality Systems]
3. **Mr. Hari Krishnan [B. E. Electronics & Instrumentations – 2016]**
   [Area: Mixed Criticality Systems]
4. **Ms. Kajal Varma [B. E. Computer Science – 2015]**
   [Area: Predictable Memory for Real-Time Systems]
5. **Mr. Sreejith V [B. E. Computer Science – 2015]**
   [Area: DVS/DFS Scheduling for MC/MP]
6. **Mr. Anurag Kashyap [B. E. Computer Science – 2015]**
   [Area: Predictable Memory for Real-Time Systems]
7. **Mr. Bharat Reddy Karka [B. E. Computer Science – 2015]**
   [Area: File Systems for Real-time Systems]
8. **Mr. Suhas Reddy [B. E. Computer Science – 2015]**
   [Area: Predictable Memory for Real-Time Systems]
9. **Mr. Rajat Jain [B. E. Computer Science – 2015]**
   [Area: DVS/DFS Scheduling for MC/MP]

10. **Mr. Shubham Kankaria [B. E. Computer Science – 2015]**
    [Area: DVS/DFS Scheduling for MC/MP]
11. **Mr. Abhinav Mehta [B. E. Computer Science – 2014]**
    [Area: DVS/DFS Scheduling for MC/MP]
12. **Mr. Pranav Pathak [B. E. Computer Science – 2014]**
    [Area: Storage Systems]
13. **Mr. Athma M Ram** [**B. E. Computer Science – 2014]**
    [Area: Social Networking using P2P]
14. **Ms. Cheruvu Alekhya [B. E. Computer Science – 2014]**
    [Area: File Systems for Flash Devices]
15. **Mr. Rakesh Vaddadi [B. E. Computer Science – 2014]**
    [Area: MC / MP Load balancing]
16. **Mr. Nishant Budhdev [MSc.Tech Information Systems – 2014]**
    [Area: Cache Coherency in MC with Quickpath]
17. **Mr. Anand Goyal [MSc. Tech Information Systems – 2014]**
    [Area: Energy Efficient Cache Architecture]
18. **Mr. Sahil Deshpande [B. E. Computer Science – 2013]**
    [Area: DVS/DFS Scheduling for Periodic Hard Real-time tasks]
19. **Mr. Chaitanya Datye [MSc. Tech Information Systems – 2013]**
    [Area: DVS/DFS Scheduling for Periodic Hard Real-time tasks]
20. **Ms. Shweta Suman [B. E. Computer Science – 2013]**
    [Area: DVS/DFS Scheduling for Aperiodic tasks]
21. **Mr. J. Pruthvi Raj [M. E. Software Systems – 2013]**
    [Area: File Systems for Flash Devices]
22. **Mr. Parag Panda [B. E. Computer Science – 2012]**
    [Area: Energy Efficient Cache Design for Embedded Systems]
23. **Ms. Sruthi Sindhura Karaturi [B. E. Computer Science – 2012]**
    [Area: Energy Efficient Cache Replacement Strategies]
24. **Mr. Akshay Goel [B. E. Computer Science – 2012]**
    [Area: Load balancing in Linux Scheduler]
25. **Ms. Meghna Mehta [B. E. Computer Science – 2012]**
    [Area: Energy Efficient Cache Design for Embedded Systems]
26. **Ms. Neethu Bal Mallya [B. E. Electronics & Instrumentation – 2012]**
    [Area: Process Aware Cache Design for Embedded Systems]
27. **Mr. Alok Upadhyay [MSc. Tech Information Systems – 2012]**
    [Area: Social Networking using P2P]

28.Ms. Prashasti Baid [B. E. Computer Science – 2011]
[Area: Modified LLF Scheduler with Reduced Preemptions]
29.Ms. Charu Gupta [B. E. Computer Science – 2011]
[Area: ARM Architecture]
30.Mr. Nagaraju Bhanoori [B. E. Computer Science – 2011]
[Area: Energy Efficient Storage Systems]
31.Mr. Prachetaa R [B. E. Computer Science – 2011]
[Area: Energy Efficient Predictive cache Architecture]
32.Mr. Kedar Soparkar [B. E. Computer Science – 2011]
[Area: Scheduling Algorithms for Real-time Systems]
33.Ms. Shivangi Singh [B. E. Computer Science – 2011]
[Area: Flash File Systems for Embedded Devices]
34.Mr. Siddharth Mohan Misra [B. E. Computer Science – 2011]
[Area: Scheduling Algorithms for Real-time Systems]
35. Mr. B. Harish Kumar [M. E. Software Systems – 2011]
[Area: Scheduling Algorithms for Real-time Systems]
36.Mr. T. Chandra Sekhar [MSc. Tech Information Systems – 2010]
[Area: Scheduling Algorithms for Real-time Systems]
37.Mr. Rajesh Somavarapu [MSc. Tech Information Systems – 2010]
[Area: Load balancing in Linux Scheduler]
38.Mr. R. Balakrishnan [B. E. Computer Science – 2010]
[Area: Flash File Systems for Embedded Devices]
39.Mr. Deepak R [M. E. Embedded Systems – 2010]
[Area: Flash File Systems for Embedded Devices]
40. Ms. Pallavi Pant [MSc. Tech Information Systems – 2008]
[Area: Real – time Scheduling Algorithm with Reduced Cache Impact]
41.P R K Sandeep [MSc. Tech Information Systems – 2008]
[Area: Real – time Scheduling Algorithm with Reduced Preemptions]

Courses Delivered to Industry for Faculty of Other Industries

1. Operating Systems for Work Integrated Learning Programmes
2. Software for Embedded Systems for Work Integrated Learning Programmes
3. Designed and Developed Course Content [Video lectures, Work sheets, Tutorials etc..] for Systems Programming course.

Professional Recognition:

1. Microsoft Young Faculty Award in the year 2009
2. Microsoft Research India Fellowship in the year 2005

Invited Talks:

1. Delivered a talk on “Energy Efficient File System for Flash Devices” for IBM Technology Day, September 17, 2007.

Membership of Professional Societies:

1. Member of IEEE and its Computer Society